In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Withdrawn) A method for developing a design of an integrated circuit, said method comprising steps of

selecting a smallest chip image from among a plurality of chip images that can supply at least a required number of I/O cells,

determining a number of excess I/O kernels of said smallest chip image in excess of said required number of I/O cells,

computing a number of other cells types which can be provided by the core area of the image and the area of the excess I/O kernels, and

evaluating from a result of said computing step if a required number of cells for said integrated circuit design can be provided within said smallest chip image if said excess I/O cells or I/O kernels are depopulated from said smallest chip image.

2. (Withdrawn) A method as recited in claim 1, wherein, if the required number of cells for said integrated circuit design can not be provided, said method includes the further step of selecting a next larger chip size and repeating said determining computing and evaluating steps.

3. (Withdrawn) A method as recited in claim 1, including the further step of selecting a smallest package size providing said required number of I/O cells and said step of selecting a smallest chip image is performed by selection from chip images corresponding to said smallest package size.

4. (Withdrawn) A method as recited in claim 2, including the further step of selecting a smallest package size providing said required number of I/O cells and said step of selecting a smallest chip image is performed by selection from chip images corresponding to said smallest package size.

5. (Withdrawn) A method as recited in claim 4, including the further step of determining, when a said larger chip size can provide said required number of cells, performing the further step of

determining if said larger chip size can be accommodated by said package and, if not, selecting a larger package size.

6. (Currently Amended) An integrated circuit including

an array of I/O kernels, each I/O kernel having a plurality of contiguous I/O cells having off-chip connections sites, said off-chip connection sites including common power connections for all I/O cells in an I/O kernel, said common power connections for an I/O kernel being independent of any other I/O kernel, ~~and~~

a plurality of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel in a standard pattern of I/O cells and having core cells formed therein, said depopulated I/O cell sites having off-chip connection sites corresponding to some off-chip connection sites of said I/O cells.

7. (Original) An integrated circuit as recited in claim 6, further including some off-chip connection pads corresponding to I/O cells in said depopulated I/O cell sites.

8. (Original) An integrated circuit as recited in claim 7, further including all off-chip connection pads corresponding to I/O cells in said depopulated I/O cell sites.

9. (Original) An integrated circuit as recited in claim 6, wherein said I/O kernels are arranged with substantially radial symmetry along edges of a semiconductor chip.

10. (Currently Amended) An integrated circuit as recited in claim 6, wherein said plurality of contiguous depopulated I/O cell sites ~~corresponding~~ correspond to an area of a said I/O kernel ~~include~~ including a corner kernel.

11. (Currently Amended) An integrated circuit as recited in claim 6, wherein said plurality of contiguous depopulated I/O cell sites ~~corresponding~~ correspond to an area of a said I/O kernel ~~include~~ including an edge kernel.

12. (Original) An integrated circuit as recited in claim 6, including at least two pluralities of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel on a single edge of a chip, said two pluralities of contiguous depopulated I/O cell sites being separated by an I/O kernel.

13. (Original) An integrated circuit as recited in claim 6, further including

a metal power connection through a said depopulated I/O cell site.

14. (Currently Amended) An integrated circuit having peripheral connections pads including

I/O cells associated with a contiguous plurality of said connection pads in a standard pattern of I/O cells and a plurality of contiguous depopulated I/O cell sites associated with a contiguous plurality of other ~~of~~ said connection pads, said depopulated I/O cells sites corresponding to areas in said standard pattern from which I/O cells have been depopulated, and

power connections ~~to~~ connecting said other connection pads and logic cells located in said depopulated I/O cell sites.